



AMENDMENTS TO THE CLAIMS

1. (Previously Presented) An integrated circuit for differential variable capacitors, comprising:

a p-substrate;

an n-well region, disposed at the top surface of said p-substrate;

at least three n-type ion implant regions, each disposed on the top surface of said n-well region;

a metal wire, for connecting said at least three n-type ion implant regions;

a bias voltage control terminal, coupled to said at least three n-type ion implant regions;

a first gate on the n-well region, said first gate being disposed on a first side of said bias voltage control terminal; and

a second gate on the n-well region, said second gate being disposed on a second side of said bias voltage control terminal opposite to said first side, said first gate and said second gate being disposed symmetrically to said bias voltage control terminal.

2. (Cancelled)

3. (Original) The integrated circuit for differential variable capacitors of claim 1, wherein said first gate is made of a polysilicon.

4. (Original) The integrated circuit for differential variable capacitors of claim 1, wherein said second gate is made of a polysilicon.

5. (Original) The integrated circuit for differential variable capacitors of claim 1, wherein said p-substrate further comprises a p-type ion implant region arranged at the top surface thereof.

6. (Original) The integrated circuit for differential variable capacitors of claim 1, wherein said p-type ion implant region is coupled to a grounding terminal.

7. (Currently Amended) An integrated circuit for differential variable capacitors, comprising:

an n-type substrate;

a ~~p-type well~~p-well region, disposed on the top surface of said n-type substrate;

at least three p-type ion implant regions, each disposed on the top surface of said ~~p-type well~~p-well region;

a metal wire, for connecting said at least three p-type ion implant regions;

a bias voltage control terminal, coupled to said at least three p-type ion implant regions;

a first gate on the p-well region, said first gate being disposed on a first side of said bias voltage control terminal; and

a second gate on the p-well region, said second gate being disposed on a second side of said bias voltage control terminal opposite to said first side, said first gate and said second gate being disposed symmetrically to said bias voltage control terminal.

8. (Cancelled)

9. (Original) The integrated circuit for differential variable capacitors of claim 7, wherein said first gate is made of a polysilicon.

10. (Original) The integrated circuit for differential variable capacitors of claim 7, wherein said second gate is made of a polysilicon.

11. (Original) The integrated circuit for differential variable capacitors of claim 7, wherein said n-type substrate further comprises an n-type ion implant region arranged at the top surface thereof.

12. (Original) The integrated circuit for differential variable capacitors of claim 11, wherein said n-type ion implant region is coupled to a grounding terminal.